**Project Workout:**

Project: 15-bit single cycle cpu.

Submitted by:

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**Instructions**: load, store, addition, substraction, multiplication, xor, beq.

**R-Type Instruction:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Opcode (3 bit) | rs (3 bit) | rt (3 bit) | rd (3 bit) | funct (3 bit) |

Instructions: addition, substraction, multiplication, division, xor.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Instructions | Hexadecimal  Instruction | Opcode | Rs | Rt | Rd | Function |
| Add | 04a0 | 000 | 010 | 010 | 100 | 000 |
| Substract | 0891 | 000 | 100 | 010 | 010 | 001 |
| Multiplication | 04a2 | 000 | 010 | 010 | 100 | 010 |
| Xor | 0653 | 000 | 011 | 001 | 010 | 011 |

**I-Type Instruction:**

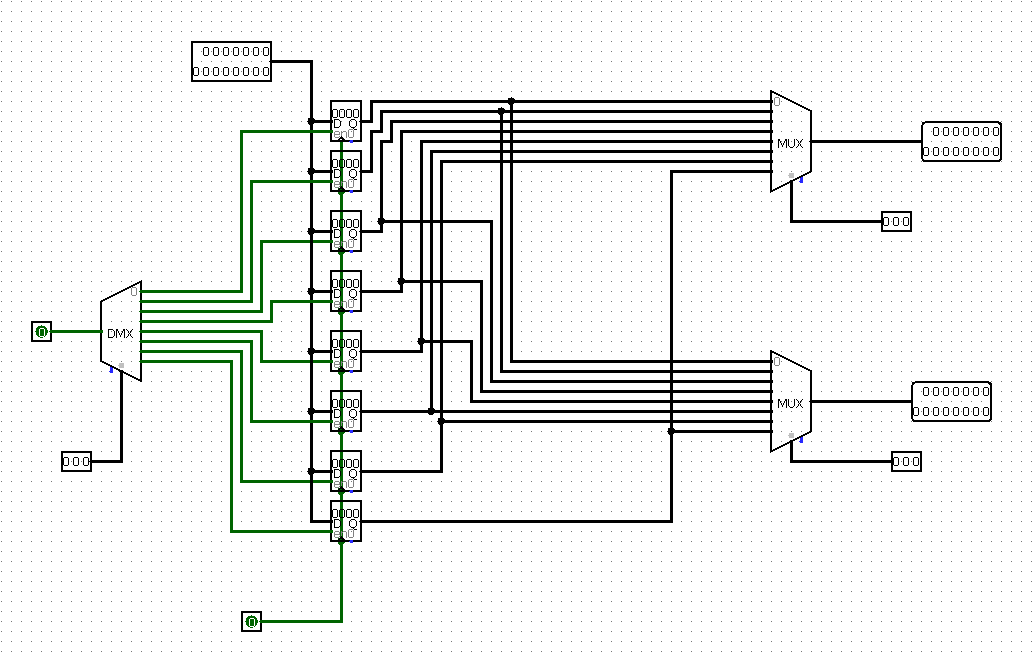
|  |  |  |  |
| --- | --- | --- | --- |
| Opcode (3 bit) | rs (3 bit) | rt (3 bit) | Immediate (6 bit) |

Instructions: load, store, beq

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Instruction | Hexadecimal  Instruction | Opcode (3) | Rs (3) | Rt (3) | Immediate (6) |
| Load | 1283 | 001 | 001 | 010 | 000011 |
| Store | 2681 | 010 | 011 | 010 | 000001 |
| beq | 34c2 | 011 | 010 | 011 | 000010 |

**Register file**:

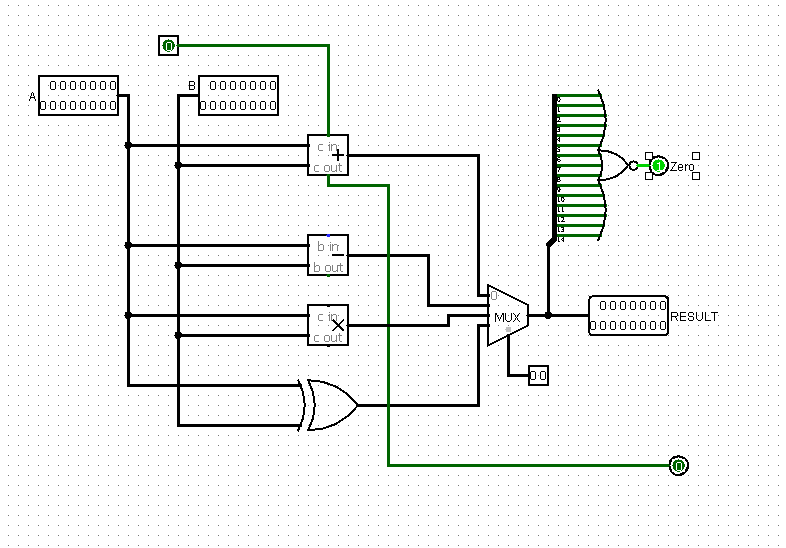
Number of Registers for register file: 8



: Image of Register file

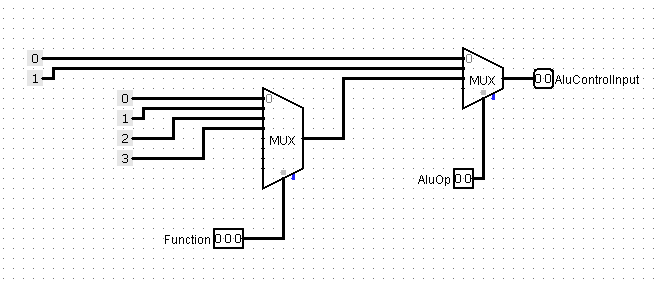
**15 Bit ALU:**

|  |  |
| --- | --- |
| Instructions | Alu Control |
| Add | 00 |
| Sub | 01 |
| Mul | 10 |
| Xor | 11 |

: Image of 15-bit alu

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Instruction Operation | AluOp1 | AluOp2 | Fun1 | Fun2 | Fun3 | ALU Control  Input1 | ALU Control  Input2 |
| LW | Load word | 0 | 0 | x | x | x | 0 | 0 |
| SW | Store word | 0 | 0 | x | X | x | 0 | 0 |
| Beq | Branch eq | 0 | 1 | X | x | x | 0 | 1 |
| R-type | Add | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| R-type | Sub | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| R-type | Mul | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| R-type | xor | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

**ALU CONTROL**

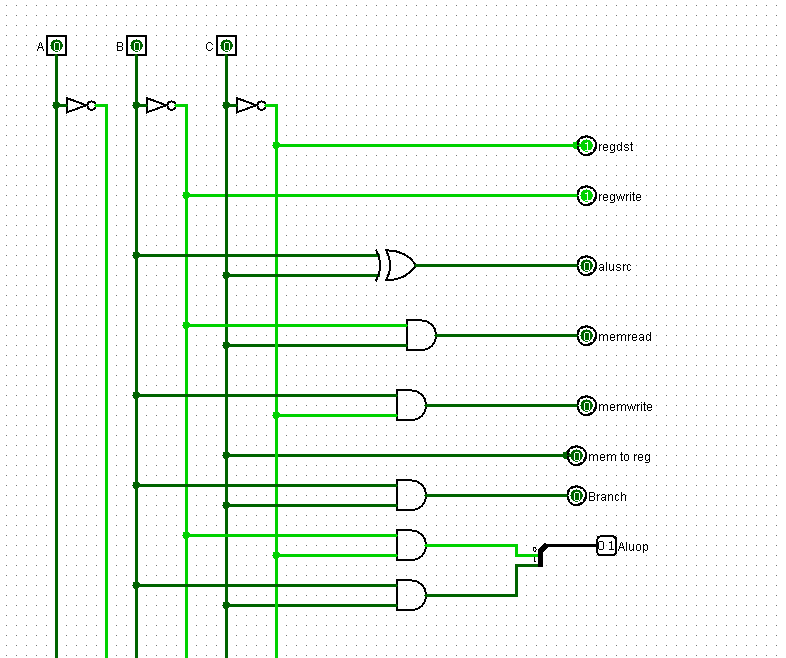


: image of ALU control circuit

**CONTROL UNIT:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Opcode | RegDst | AluOp1 | AluOp2 | ALUSrc | Branch | MemRead | MemWrite | Regwrite | Memto Reg |
| R-format | 000 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Lw | 001 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| Sw | 010 | X | 0 | 0 | 1 | 0 | 0 | 1 | 0 | X |
| beq | 011 | x | 0 | 1 | 0 | 1 | 0 | 0 | 0 | X |

1:Control unit



: Image of control unit circuit

**Datapath:**

